

OM6221 BLE Register Map

Version 0.7

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Revision History

Revision	Date	Description
V0.1	Sep 4, 2025	Initial draft
V0.2	Sep 11, 2025	Update power domain of register
V0.3	Nov 21, 2025	Add GPIO2 and GPIO1 Update GPIO MISO IRQ default value Remove pd_Idx33_mn and pd_Idx33_reg
V0.4	Dec 19, 2025	Update EXT_IO_INOUT and EXT_IO_CTL
V0.5	Dec 23, 2025	Update BLE_CRC_INT
V0.6	Jan 22, 2025	Update default value of CONFIG_EXT
V0.7	Feb 11, 2025	Add description of some registers after entering PowerDown mode

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Register Definition

BANK0

CONFIG (RW) Address: 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MASK_EVT_DS	MASK_RX_DR	MASK_TX_DS	MASK_SYNC_DS	EN_CRC	CE_REG	PWR_UP	Event_abort_dis
1	0	0	0	1	0	0	1
RW	RW	RW	W	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
7	0	MASK_EVT_DS	Mask event interrupt by Event_Done
			0 Reflect Event_Done as active low interrupt on the IRQ pin
			1 Interrupt not reflected on the IRQ pin
6	0	MASK_RX_DR	Mask interrupt caused by RX_DR
			0 Reflect RX_DR as active low interrupt on the IRQ pin
			1 Interrupt not reflected on the IRQ pin
5	0	MASK_TX_DS	Mask interrupt caused by TX_DS
			0 Reflect TX_DS as active low interrupt on the IRQ pin
			1 Interrupt not reflected on the IRQ pin
4	0	MASK_SYNC_DS	Mask interrupt caused by sync detector
			0 Reflect SYNC_DS as active low interrupt on the IRQ pin
			1 Interrupt not reflected on the IRQ pin
3	1	EN_CRC	Enable CRC. Forced high if one of the bits in the EN_AA is high
			0 Disable CRC
			1 Enable CRC
2	0	CE_REG	CE controlled by register
			0 CE low
			1 CE high
1	0	PWR_UP	Power up control
			0 POWER DOWN
			1 POWER UP
0	1	Event_abort_dis	Event_abort_disable
			0 Event abort enable
			1 Event abort disable

EN_AA (RW) Address: 01h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reversed			RTC_LCK	Reserved	Reserved	Reserved	Event_abort_en_bar
0			0	0	1	1	1
RW			R	R	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
7:5	3'h0	Reserved	
4	0	RTC_LCK	
3:1	3'h3	Reserved	
0	1	Event_abort_en_bar	Event_abort_en_bar
			0 Event abort
			1 Not abort

EN_RXADDR (RW) Address: 02h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reversed			RXMD_EN	scramble_en	ERX_P2	ERX_P1	ERX_P0
0			0	1	0	1	1
RW			RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
7:5	0	Reserved	
4	0	RXMD_EN	RXMD enable
3	1	scramble_en	Scramble enable
			0 Disable
			1 Enable
2	0	ERX_P2	Enable data pipe 2
			0 Disable
			1 Enable
1	1	ERX_P1	Enable data pipe 1
			0 Disable
			1 Enable

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0	1	ERX_P0	Enable data pipe 0	
			0	Disable
			1	Enable

PMU_CTL (RW) Address: 03h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rtc32k_rdy_enb_reg	Rtc32k_rdy_enb_mn	Digldo_enb_dly_reg	Digldo_enb_mn	Digldo_enb_reg	rtc32k_en	RF_PWRDWN[1:0]	
1	0	1	0	1	0	01	
RW	RW	RW	RW	RW	RW	RW	

Description of Word

Bit	Value	Symbol	Description
7	1	Rtc32k_rdy_enb_reg	For debug mode
6	0	Rtc32k_rdy_enb_mn	Rtc32k manual mode select, 0 for fsm control; 1 for manual mode
5	1	Digldo_enb_dly_reg	For debug mode
4	0	Digldo_enb_mn	Digital ldo manual mode select, 0 for fsm control; 1 for manual mode
3	1	Digldo_enb_reg	For debug mode
2	0	rtc32k_en	Rtc32k enable, 0 for disable; 1 for enable, BLE mode should be set 1
1:0	2'b01	RF_PWRDWN[1:0]	Working mode select 00 active mode 01 deep sleep mode 10 light sleep mode

SETUP_RETR (RW) Address: 04h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Alarm2tim							
0x03							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	0x03	Alarm2tim	Alarm2 time setting
		8'hff	255 cycles of rtc32k

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			...	...
			4'h01	1 cycle of rtc32k
			4'h00	Now

RF_CH (RW) Address: 05h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reg_Rf_ch							
0x32							
RW							

Description of Word

Bit	Value	Symbol	Description
8:0	2	Reg_Rf_ch	Set the frequency channel

RF_SETUP (RW) Address: 06h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONT_WAVE	PA_PWR[3]	CAL_DONE	CAL_EN	RF_DR_HIGH	Pa_power		
0	1	0	1	0	3'b000		
RW	RW	RW	RW	RW	RW		

Description of Word

Bit	Value	Symbol	Description
7	0	CONT_WAVE	Enables continuous carrier transmit when high
			0 Disable
			1 Enable
6	1	PA_PWR[3]	PA power select bit 3
5	0	CAL_DONE	Flag for calibration finishing, after CAL_EN set to 1, CAL_DONE will be reset to 0 0 calibration on 1 calibration done
4	0	CAL_EN	Calibration enable, 1 for enable; 0 for disable. After calibration done, CAL_EN will be reset to 0 by hardware. Users don't need to configure CAL_EN=0.
3	1	RF_DR_HIGH	Data rate select, 1 for 2Mbps; 0 for 1Mbps, BLE mode should be set to 0
2:0	3'b010	PA_PWR[2:0]	PA power control, PA_PWR[3:0] with pa_voltage of RF_IVGEN in bank1

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PA_PWR[3:0]	Pa_voltage(bank1 of RF_IVGEN)	
1111	0	Output 8dbm,
1000	0	Output 5 dbm
0111	1	Output 4dbm,
0011	0	Output 0 dbm,
0001	0	Output -6 dbm
0001	1	Output -12 dbm
0000	0	Output -32 dbm
0000	1	Output -43 dbm

STATUS (RW) Address: 07h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BANK	RX_DR	TX_DS	SYNC_DS	TIMER_INT_STATUS	RX_TIMEOUT_INT	EVENT_DONE	TX_FULL
0	0	0	0	0	0	0	0
R	RW	RW	RW	R	R	R	R

Note: OM6221 works in 2.4G mode by default. Default value of bit2~1 is 2'b11. After enabling BLE mode, default value of bit2~1 will be changed to 2'b00.

Description of Word

Bit	Value	Symbol	Description
7	0	BANK	Register BANK status
			1 Register R/W is to register BANK1
			0 Register R/W is to register BANK0
6	0	RX_DR	Data Ready RX FIFO interrupt. Asserted when new data arrives RX FIFO Write 1 to clear bit.
5	0	TX_DS	Data Sent TX FIFO interrupt. Asserted when packet transmitted on TX. Write 1 to clear bit.
4	0	SYNC_DS	RX sync detector interrupt, Write 1 to clear bit. If SYNC_DS is asserted it must be cleared to enable further communication.
3	0	TIMER_INT_STATUS	Timer interrupt status
			1 Timer interrupt is assert
			0 Timer interrupt is not assert
2	0	RX_TIMEOUT_INT	RX timeout status
			1 RX timeout interrupt is assert
			0 RX timeout interrupt is not assert
1	0	EVENT_DONE	Event done status
			1 Event is done

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			0	Event is not done
0	0	TX_FULL	TX FIFO full flag	
			0	Available locations in TX FIFO
			1	TX FIFO full

TX HEADER1 (RW) Address: 09h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
length							
0							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rxadd	Txadd	RFU		TYPE			
0	0	0		0			
RW	RW	RW		RW			

Description of Word

Bit	Value	Symbol	Description
15:8	8'h00	length	Payload length
7	0	Rxadd	0 for device RX address 1 for random address
6	0	Txadd	0 for device TX address 1 for random address
5:4	2'h0	RFU	Reserved
3:0	4'h0	TYPE	0000 ADV_IND 0001 ADV_DIRECT_IND 0010 ADV_NONCONN_IND 0100 SCAN_RSP 0110 ADV_SCAN_IND 0111-1111 RESERVED

BLE_ACCESS_ADDR (RW) Address: 0Ah

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
BLE_ACCESS_ADDR							
8'h8e							

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RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
BLE_ACCESS_ADDR							
8'h89							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
BLE_ACCESS_ADDR							
8'hbe							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BLE_ACCESS_ADDR							
8'hd6							
RW							

Description of Word

Bit	Value	Symbol	Description
31:0	32'h8e89 bed6	BLE_ACCESS_ADDR	BLE access address

BLE_TIMER (RW) Address: 0Bh

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Ble_timer[31:24]							
8'h00							
RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Ble_timer[23:16]							
8'h00							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Ble_timer[15:8]							
8'h00							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ble_timer[7:0]							
8'h00							
RW							

Description of Word

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Bit	Value	Symbol	Description
31:0	32'h000 000c2	Ble_timer	BLE timer

BLE_CTL (RW) Address: 0Ch

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
event_abort	md_dsb	nesn_sn_dsb	infiniterx	FORMAT			
1	1	0	0	4'h3			
RW	RW	RW	RW	RW			

Description of Word

Bit	Value	Symbol	Description
7	1	event_abort	Event abort by software
6	1	md_dsb	Md disable
5	0	nesn_sn_dsb	Nesn and sn disable
4	0	infiniterx	Infinite RX
3:0-	4'h3	FORMAT	0011 for BLE broadcast 0101 for BLE connection 0110 for BLE normal scan mode 0111 for BLE white list filter mode 1001 for BLE TX test 1011 for BLE RX test

CLKN_SYNC Address: 0Dh

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
CLKN_SYNC[31:24]							
8'h00							
R							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
CLKN_SYNC [23:16]							
8'h00							
R							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CLKN_SYNC [15:8]							
8'h00							
R							

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Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKN_SYNC[7:0]							
8'h00							
R							

Description of Word

Bit	Value	Symbol	Description
31:0	32'h00000000	CLKN_SYNC	Latch 32k timer counter when sync detect

EXT_IO_INOUT Address: 0Eh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	miso_reg	irq_reg	gpio_reg[2:0]		
0	0	0	0	0	3'b000		
R	R	R	RW	RW	RW		

Description of Word

Bit	Value	Symbol	Description
7	0	Reserved	
6	0	Reserved	
5	0	Reserved	
4	0	miso_reg	When SPI read from MISO pad, miso_reg = miso_reg_out; when SPI write to MISO pad, miso_reg = miso_reg_in
3	0	irq_reg	When SPI read from IRQ pad, irq_reg = irq_reg_out; when SPI write to IRQ pad, irq_reg = irq_reg_in
2:0	3'b000	gpio_reg[2:0]	When SPI read from GPIO[2:0] pad, gpio_reg[2:0] = gpio_reg_out[2:0]; when SPI write to GPIO[2:0] pad, gpio_reg[2:0] = gpio_reg_in[2:0]

EXT_IO_CTL Address: 0Fh

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Reserved						mosi_drv	miso_drv
6'h00						0	0
R						RW	RW
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
irq_drv	gpio_drv	miso_oe	irq_oe	gpio_oe[2:0]		irq_sel	
0	0	0	0	3'b000		1	
RW	RW	RW	RW	RW		RW	

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Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
miso_pd_en	irq_pd_en	gpio_pd_en[2:0]			miso_wk_en	irq_wk_en	gpio_wk_en[2]
1	0	3'b111			0	0	0
RW	RW	RW			RW	RW	RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
gpio_wk_en[1:0]		mosi_pu_en	miso_pu_en	irq_pu_en	gpio_pu_en[2:0]		
2'b00		0	0	0	3'b000		
RW		RW	RW	RW	RW		

Description of Word

Bit	Value	Symbol	Description
31:26	6'h00	Reserved	
25	0	mosi_drv	MOSI output driving capability
24	0	miso_drv	MISO output driving capability
23	0	irq_drv	IRQ output driving capability
22	0	gpio_drv	GPIO output driving capability
21	0	miso_oe	Output enable during MISO is used as extension IO
20	0	irq_oe	Output enable during IRQ is used as extension IO
19:17	3'b000	gpio_oe[2:0]	Output enable of GPIO
16	1	irq_sel	irq_sel=0, IRQ is used as extension IO; irq_sel=1 IRQ is used as interrupt
15	1	miso_pd_en	150k pull down enable of MISO
14	0	irq_pd_en	150k pull down enable of IRQ
13:11	3'b111	gpio_pd_en[2:0]	150k pull down enable of GPIO
10	0	miso_wk_en	Wake up enable of MISO for extension IO
9	0	irq_wk_en	Wake up enable of IRQ for extension IO
8:6	3'b000	gpio_wk_en[2:0]	Wake up enable of GPIO for extension IO
5	0	mosi_pu_en	150k pull up enable of MOSI
4	0	miso_pu_en	150k pull up enable of MISO
3	0	irq_pu_en	150k pull up enable of IRQ
2:0	3'b000	gpio_pu_en[2:0]	150k pull up enable of GPIO

TX_ADVA(RW) Address: 10h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit47	Bit46	Bit45	Bit 44	Bit43	Bit 42	Bit41	Bit 40
TX_ADVA							
8'h70							

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RW							
Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
TX_ADVA							
8'h70							
RW							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
TX_ADVA							
8'h41							
RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
TX_ADVA							
8'h88							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TX_ADVA							
8'h20							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX_ADVA							
8'h46							
RW							

Description of Word

Bit	Value	Symbol	Description
47:0	48'h707 0418820 46	TX_ADVA	BLE device address

TX HEADER (RW) Address: 11h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
length							
0							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rxadd	Txadd	RFU		TYPE			
0	0	0		0			
RW	RW	RW		RW			

Description of Word

Bit	Value	Symbol	Description
15:8	2'b00	length	Payload length
7	0	Rxadd	0 for device RX address 1 for random address
6	0	Txadd	0 for device TX address 1 for random address
5:4	2'h0	RFU	Reserved
3:0	4'h0	TYPE	0000 ADV_IND 0001 ADV_DIRECT_IND 0010 ADV_NONCONN_IND 0100 SCAN_RSP 0110 ADV_SCAN_IND 0111-1111 RESERVED

BLE_CRC_INIT (RW) Address: 12h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Ble_crc_init[23:16]							
8'h55							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Ble_crc_init[15:8]							
8'h55							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ble_crc_init[7:0]							
8'h55							
RW							

Description of Word

Bit	Value	Symbol	Description
23:0	24'h555 555	Ble_crc_init	Ble CRC initial value

BLE_SETUP_DELAY (RW) Address: 13h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ble_tx_delay[3:0]				Ble_rx_delay[3:0]			
0				0			
RW				RW			

Description of Word

Bit	Value	Symbol	Description
7:4	0	Ble_tx_delay	0000 no delay 0001 1us delay 0010 2us delay 0011 3us delay 0100 4us delay 0101 5us delay 0110 6us delay 0111 7us delay 1000 0us delay 1001 -1us delay 1010 -2us delay 1011 -3us delay 1100 -4us delay 1101 -5us delay 1110 -6us delay 1111 -7us delay

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3:0	0	Ble_rx_delay	0000 no delay 0001 1us delay 0010 2us delay 0011 3us delay 0100 4us delay 0101 5us delay 0110 6us delay 0111 7us delay 1000 0us delay 1001 -1us delay 1010 -2us delay 1011 -3us delay 1100 -4us delay 1101 -5us delay 1110 -6us delay 1111 -7us delay
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RX HEADER(R) Address: 14h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 15	Bit 14	Bit 13	Bit 12	Bit11	Bit 10	Bit 9	Bit 8
length							
0							
R							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rxadd	Txadd	RFU		TYPE			
0	0	0		0			
R	R	R		R			

Description of Word

Bit	Value	Symbol	Description
15:8	8'h00	length	Payload length
7	0	Rxadd	0 for device RX address 1 for random address
6	0	Txadd	0 for device TX address 1 for random address
5:4	2'h0	RFU	Reserved
3:0	4'h0	TYPE	0011 SCAN_REQ 0101 CONNECT_REQ 0111-1111 RESERVED

RX_ADDA(R) Address: 15h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit47	Bit46	Bit45	Bit 44	Bit43	Bit 42	Bit41	Bit 40
RX_ADDA							
8'h0							
R							
Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
RX_ADDA							
8'h0							
R							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
RX_ADDA							
8'h0							
R							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
RX_ADDA							
8'h0							
R							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
RX_ADDA							
8'h0							
R							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDA							
8'h0							
R							

Description of Word

Bit	Value	Symbol	Description
47:0	48'h0	RX_ADDA	Peer device address

RX_STATUS (RW) Address: 16h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CS_NEW_L ASTEMPTY	NEW_LAST _EMPTY	SNERR	NESNERR	CRCERR	LENERR	TYPEERR	SYNCERR

OM6221 BLE Register Map v0.7

0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

Description of Word

Bit	Value	Symbol	Description
7	0	CS_NEW_LAS EMPTY	
6	0	NEW_LAST_E MPTY	Last packet is empty
5	0	SNERR	Sn error, if rxsn is not equal with the txsn, the duplication detect
4	0	NESNERR	Nesn error, if rxnesn equals txsn, then NACK detect.
3	0	CRCERR	Crc error
2	0	LENERR	Lenth error. Advertiser: If rxtype is SCAN_REQ, packet's length is not longer than 12 bytes; If rxtype is CONNECT_REQ, packet's length is no longer than 34 bytes Scanner or rf_test The packet's length is no longer than 37 bytes Connect data packet's length is no longer than 31 bytes
1	0	TYPEERR	Type error. The tx type of device should be matched with the rxtype received Advertiser: Txtype is ADV_IND, rxtype should be SCAN_REQ or CONNECT_REQ; Txtype is ADV_SCAN_IND, rxtype should be SCAN_REQ; Txtype is ADV_DIRECT_IND, rxtype should be CONNECT_REQ; Scanner: Rxtype should be ADV_IND, ADV_DIRE_IND, ADV_SCAN_IND, ADV_NOCON_IND; If device is passive scanner, after transmit scan_req, SCAN_RSP can be received
0	0	SYNCERR	Sync error, when rx time out, syncerr is set.

FIFO_STATUS (RW) Address: 17h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	TX_REUSE_ PL	TX_FULL	TX_EMPTY	Reserved		RX_FULL	RX_EMPTY
0	0	0	1	0		0	1
RW	R	R	R	RW		R	R

Description of Word

OM6221 BLE Register Map v0.7

Bit	Value	Symbol	Description
7	0	Reserved	
6	0	TX_REUSE_PL	TX REUSE flag.
			1 Tx data reused
			0 Tx data not reused
5	0	TX_FULL	TX FIFO full flag.
			1 TX FIFO full
			0 Available locations in TX FIFO
4	1	TX_EMPTY	TX FIFO empty flag.
			1 TX FIFO empty
			0 Data in TX FIFO
3:2	2'b00	Reserved	Only '00' allowed
			0 Keep the current value
			1 Reset to default values
1	0	RX_FULL	RX FIFO full flag.
			1 RX FIFO full
			0 Available locations in RX FIFO
0	1	RX_EMPTY	RX FIFO empty flag.
			1 RX FIFO empty
			0 Data in RX FIFO

CONFIG_EXT (RW) Address: 18h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
clk_rx_en	ce_before_fifo	rxfifo_mx	Msk_rx_time_out	Reserved	Reserved	Msk_rtc_time_r_int	ble_timer_on
0	0	0	1	0	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
7	0	clk_rx_en	RX clock enable
6	0	ce_before_fifo	
5	0	rxfifo_mx	Use RX FIFO as 2nd TX FIFO 1: RX FIFO is used as 2nd TX FIFO 0: RX FIFO is used as RX FIFO
4	1	Msk_rx_time_out	Mask RX time out
3	0	Reserved	
2	0	Reserved	
1	1	Msk_rtc_timer_int	Mask rtc timer interrupt

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0	0	ble_timer_on	Blrtc timer enable
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RTC_TIMER_MODE (RW) Address: 19h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				Alarm1_wkrf_en	Wake_up_ctrl	Rtc_mode	
4'h0				0	0	2'b00	
RW				RW	RW	RW	

Description of Word

Bit	Value	Symbol	Description
7:4	4'h0	Reserved	
3	1'b0	Alarm1_wkrf_en	Enable alarm1 to assert CE 0: not allow alarm1 to assert CE 1: allow alarm1 to assert CE
2	1'b0	Wake_up_ctrl	Sleep timer wake up control 0: generate wake up interrupt when CPU is not sleep 1: generate wake up interrupt no matter CPU is in sleep or not
1:0	2'b00	Rtc_mode	2'b00: set absolute value; read rtc timer value, soft first send lock cmd and wait lock done 2'b10: set delta value; soft need not read rtc timer value 2'bx1: set absolute value; read rtc timer value, soft need not wait

WHITE_LIST_RXADDR_1 (RW) Address: 1Ah

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit47	Bit46	Bit45	Bit 44	Bit43	Bit 42	Bit41	Bit 40
WHITE_LIST_RXADDR_1							
8'h0							
RW							
Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
WHITE_LIST_RXADDR_1							
8'h0							
RW							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
WHITE_LIST_RXADDR_1							
8'h0							
RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16

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WHITE_LIST_RXADDR_1							
8'h0							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
WHITE_LIST_RXADDR_1							
8'h0							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WHITE_LIST_RXADDR_1							
8'h0							
RW							

Description of Word

Bit	Value	Symbol	Description
47:0	48'h0	WHITE_LIST_RXADDR_1	

WHITE_LIST_RXADDR_2 (RW) Address: 1Bh

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit47	Bit46	Bit45	Bit 44	Bit43	Bit 42	Bit41	Bit 40
WHITE_LIST_RXADDR_2							
8'h0							
RW							
Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
WHITE_LIST_RXADDR_2							
8'h0							
RW							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
WHITE_LIST_RXADDR_2							
8'h0							
RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
WHITE_LIST_RXADDR_2							
8'h0							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
WHITE_LIST_RXADDR_2							
8'h0							

OM6221 BLE Register Map v0.7

RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WHITE_LIST_RXADDR_2							
8'h0							
RW							

Description of Word

Bit	Value	Symbol	Description
47:0	48'h0	WHITE_LIST_RXADDR_2	

DYNPD (RW) Address: 1Ch

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Bypass_io	Xn_en	Spi4_en	DPL_P2	DPL_P1	DPL_P0
0	0	1	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
7	0	Reserved	
6	0	Reserved	
5	1	Bypass_io	Bypass IRQ and MOSI, after HS6220 power up, Bypass_io should be set 0
4	0	Xn_en	Xn mode enable
3	0	Spi4_en	4-wire SPI enable
2	0	DPL_P2	Enable dynamic payload length data pipe 2. (Requires EN_DPL and ENAA_P2)
1	0	DPL_P1	Enable dynamic payload length data pipe 1. (Requires EN_DPL and ENAA_P1)
0	0	DPL_P0	Enable dynamic payload length data pipe 0. (Requires EN_DPL and ENAA_P0)

FEATURE (RW) Address: 1Dh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
White_list_en	Ble_en	Soft_rst	BP_GAU	hw_adv	EN_DPL	EN_ACK_PAY	EN_DYN_ACK
0	0	0	1	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

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Bit	Value	Symbol	Description
7	0	White_list_en	White list enable
6	0	Ble_en	BLE mode enable
5	0	Soft_rst	Software reset
4	1	BP_GAU	Bypass Gaussian filter, BLE mode should not bypass Gaussian filter
3	0	hw_adv	Hardware auto advertise 1: enable hardware auto send advertise packet 0: disable hardware auto send advertise packet
2	0	EN_DPL	Enables Dynamic Payload Length
1	0	EN_ACK_PAY	Enables Payload with ACK
0	0	EN_DYN_ACK	Enables the W_TX_PAYLOAD_NOACK command

SETUP_VALUE (RW) Address: 1Eh

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
TX_WAIT_CNT							
8'h00							
RW							
Bit23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit17	Bit16
REG_LNA_WAIT							
8'h00							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit8
REG_MBG_WAIT							
8'h06							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit2	Bit 1	Bit 0
RX_TM_CNT							
8'h80							
RW							

Description of Word

Bit	Value	Symbol	Description
31:24	8'h00	TX_WAIT_CNT	When CE is high and TX FIFO is not empty, wait cycles to send the following packet
	8'hff		255 cycle
	...		...
	1		1 cycle
	0		0 cycle

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23:16	8'h00	REG_LNA_WA IT	Lna wait counter	
			8'hff	255 cycle
			...	...
			1	1 cycle
			0	0 cycle
15:8	8'h06	REG_MBG_W AIT	Main bandgap wait counter	
			8'hff	255us
			...	...
			1	1 us
			0	0 us
7:0	8'h80	RX_TM_CNT	Rx timeout counter.	
			8'hff	255us
			...	...
			1	1 us
			0	0 us

PRE_GURD (RW) Address: 1Fh

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
reserved							Tail_01
0							0
R							RW
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
SPARE_REG[7:2]						Pa_bias	
0						10	
RW						RW	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TAIL_CTL			GRD_EN	GRD_CNT			
011			1	4'h7			
RW			RW	RW			

Description of Word

Bit	Value	Symbol	Description
23:17	0	reserved	
16	0	Tail_01	Control tail phase to transmit 0 or 1
15:10	0	SPARE_REG	Reserved register
9:8	10	Pa_bias	00 80uA 01 60uA

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			10 40uA 11 20uA
7:5	3'h3	TAIL_CTL	Number of repeat bit after the CRC
			7 7 repeat tail
			
			1 1 repeat tail
			0 0 No repeat tail
4	1	GRD_EN	Pre-Guard enable
3:0	4'h7	GRD_CNT	Number of Pre-Guard bit before preamble
			4'hf 16 bit pre_guard
			
			1 2 bit pre_guard
			0 1 bit pre_guard

BANK1

LINE (R) Address: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CID							
8'h0c							
R							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CID							
8'h00							
R							

Description of Word

Bit	Value	Symbol	Description
15:0	16'h0c00	CID	Chip ID

PLL_CTL0 (RW) Address: 01h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode. Bit14 only supports write, does NOT support read.

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Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
SDM_EN	Pll_dac_en	PLL_RSTN_PFD	CRY_PD_REG	CRY_PD_MN	Reserved	PLL_FOFFSET_SEL	
1	1	1	0	0	0	01	
RW	RW	RW	RW	RW	RW	RW	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
DAC_CAL_EN_REG	DAC_CAL_EN_MN	DAC_CALM_ODE_REG	BP_RC_BP	DOC_CAL_EN_REG	DOC_CAL_EN_MN	DOC_DAC_MN	I_Q_RVS
0	0	0	1	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PLL_TEST_EN	pd_pkdet_reg	pd_pkdet_mn	PD_PLL_REG	PD_PLL_MN	PLL_TX_EN_REG	PLL_TX_EN_MN	BYPASS_VCO_RES
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDM_DITH_IN	SDM_DITH_EN	DAC_RANG_E_MN	SYNC_DET_DIS	AFC_EN_REG	AFC_EN_MN	CTUNING_MN	FTUNING_MN
0	1	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description	
31	1	SDM_EN	SDM enable	
			1	Enable the SDM
			0	Disable the SDM
30	1	Pll_dac_en	Output DAC_EN to analog	
			0	Output 0
			1	Output 1
29	1	PLL_RSTN_PFD	PLL_RSTN_PFD control	
			1	Set 1
			0	Set 0
28	0	CRY_PD_REG	Control the Power down of Crystal	
			1	Power down the crystal
			0	Power up the crystal
27	0	CRY_PD_MN	Select the source of crystal power down	
			1	CRY_PD = CRY_PD_REG
			0	CRY_PD = CRY_PD_FSM
26	0	Reserved		

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25:24	01	PLL_FOFFSET_SEL	PLL_FOFFSET_SEL control	
23	0	DAC_CAL_EN_REG	DAC calibration enable	
			1	Enable the DAC calibration
			0	Disable the DAC calibration
22	0	DAC_CAL_EN_MN	Select the source of DAC_CAL_EN	
			1	DAC_CAL_EN = DAC_CAL_REG
			0	DAC_CAL_EN = DAC_CAL_FSM
21	0	DAC_CALMODE_REG	Control the VCO gain	
			1	Normal gain
			0	5 times of the normal gain
20	1	BP_RC_BP	Bypass RC_BP phase in the FSM	
			1	Bypass RC_BP phase
			0	No bypass RC_BP phase
19	0	DOC_CAL_EN_REG	Enable the DOC calibration	
			1	Enable the DOC calibration
			0	Disable the DOC calibration
18	0	DOC_CAL_EN_MN	Select the source of DOC_CAL_EN source	
			1	DOC_CAL_EN = DOC_CAL_EN_REG
			0	DOC_CAL_EN = DOC_CAL_EN_FSM
17	0	DOC_DAC_MN	Select the source of DOC source	
			1	DOC_DACI = DOC_DACI_REG DOC_DACQ = DOC_DACQ_REG
			0	DOC_DACI = DOC_DACI_FSM DOC_DACQ = DOC_DACQ_FSM
16	0	I_q_rvs	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
15	0	PLL_TEST_EN	Enable the PLL in test mode	
			1	PLL A_CNT and B_CNT come from register
			0	PLL A_CNT and B_CNT come from SDM
14	0	pd_pkdet_reg	Manual mode of pd_pkdet register	
13	0	pd_pkdet_mn	Manual mode of pd_pkdet enable	
12	0	PD_PLL_REG	PLL power down control	
			1	Power down PLL
			0	Power up PLL
11	0	PD_PLL_MN	Select the source of PLL Power down	
			1	PD_PLL = PD_PLL_REG
			0	PD_PLL = PD_PLL_FSM
10	0	PLL_TX_EN_REG	PLL TX mode	
			1	PLL in TX mode

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			0	PLL in RX mode
9	0	PLL_TX_EN_MN	Select the source of PLL_TX_EN	
			1	PLL_TX_EN = PLL_TX_EN_REG
			0	PLL_TX_EN = PLL_TX_EN_FSM
8	0	BYPASS_VCO_RES	Bypass VCO tail resistor for max amplitude	
7	0	SDM_DITH_IN	SDM dither in value	
			1	Value 1
			0	Value 0
6	0	SDM_DITH_EN	SDM dither enable	
			1	Enable the SDM dither
			0	Disable the SDM dither
5	0	DAC_RANG_MN	Select the source of DAC_RANG	
			1	DAC_RANG = DAC_RANG_REG
			0	DAC_RANG = DAC_RANG_FSM
4	0	SYNC_DET_DIS	Disable AGC when sync detected	
3	0	AFC_EN_REG	AFC enable	
			1	Enable the AFC
			0	Disable the AFC
2	0	AFC_EN_MN	Select the source of AFC_EN	
			1	AFC_EN = AFC_EN_REG
			0	AFC_EN = AFC_EN_FSM
1	0	CTUNING_MN	Select the source of CTUNING	
			1	CTUNING = CTUNING_REG
			0	CTUNING = CTUNING_FSM
0	0	FTUNING_MN	Select the source of FTUNING	
			1	FTUNING = FTUNING_REG
			0	FTUNING = FTUNING_FSM

PLL_CTL1 (RW) Address: 02h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
REG_TX_PA_WAIT							
8'h10							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Tx_PLL_WAIT							
8'h42							

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RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
REG_AFC_WAIT							
8'h00							
RW							

Description of Word

Bit	Value	Symbol	Description
23:16	8'h10	REG_TX_PA_WAIT	The time between power up PA to transmit data
			8'hff 255 cycle
			
			1 1 cycle
			0 0 cycle
15:8	8'h42	Tx_PLL_WAIT	Pll lock wait time in Tx mode
			8'hff 255 us
			
			1 1 us
			0 0 us
7:0	8'h00	REG_AFC_WAIT	The time between RC done and AFC start
			8'hff 255 us
			
			1 1 us
			0 0 us

CAL_CTL (RW) Address: 03h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode. After calibration done, bp_dac and bp_vco_ldo will be set to 1 by hardware. bp_dc and bp_afc can NOT be set to 1 for RX/TX.

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Rx_pll_wait							
8'h28							
RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Pa_byps_en	afc_w_sel		Bp_calib	Bp_dc	Bp_dac	Bp_afc	Reserved
0	11		0	0	0	0	0
RW	RW		RW	RW	RW	RW	RW
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
bp_vco_ldo	Pseudo_rnd	Bp_rx_addr	Reserved	Bp_cp_diox	Vco_ldo_cal_reg		
0	0	0	0	1	0		

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WR	RW	RW	RW	RW			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Vco_ldo_cal_mn	Reserved	PlL_rst_cnt	Reserved				
0	0	1	0				
RW	RW	RW	RW				

Description of Word

Bit	Value	Symbol	Description
31:24	8'h28	Rx_pll_wait	PlL lock wait time in rx mode Force_cal : before every transmit and receive do calibration
23	0	Pa_byps_en	Bypass PA current source to enhance TX power
22:21	11	afc_w_sel	Select the AFC wait reference counter
			0 512
			1 255
			2 127
			3 63
20	0	Bp_calib	If channel is not changed, calibration step can be bypassed, 1 for bypass, 0 for not bypass
19	0	Bp_dc	Bypass DC calibration phase
			0 Disable
			1 Enable
18	0	Bp_dac	Bypass DAC calibration phase
			0 Disable
			1 Enable
17	0	Bp_afc	Bypass AFC calibration phase
			0 Disable
			1 Enable
16	0	Reserved	
15	0	bp_vco_ldo	Bypass VCO_LDO calibration phase
			0 Disable
			1 Enable
14	0	Pseudo_rnd	Transmit Random data
			0 Disable
			1 Enable
13	0	Bp_rx_addr	Bypass the RX_ADDR phase in the main FSM
12	0	Reserved	

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11	1	Bp_cp_diox	Bpassdio	
			0	Disable
			1	Enable
10:8	0	Vco_ldo_cal_reg	Vco_ldomamual set value	
7	0	Vco_ldo_cal_mn	Vcoldo calibration select	
			0	Vco_ldo_cal = vco_ldo_cal_fsm
			1	Vco_ldo_cal = vco_ldo_cal_reg
6	0	Reserved		
5	1	Pll_rst_cnt	Pll_rst_cnt	
			0	Output 0
			1	Output 1
4:0	0	Reserved		

STATUS (RW) Address: 07h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BANK	RX_DR	TX_DS	SYNC_DS	TIMER_INT_STATUS	RX_TIMEO UT_INT	EVENT_DONE	TX_FULL
0	0	0	0	0	0	0	0
R	RW	RW	RW	R	R	R	R

Note: OM6221 works in 2.4G mode by default. Default value of bit2~1 is 2'b11. After enabling BLE mode, default value of bit2~1 will be changed to 2'b00.

Description of Word

Bit	Value	Symbol	Description
7	0	BANK	Register BANK status
			1 Register R/W is to register BANK1
			0 Register R/W is to register BANK0
6	0	RX_DR	Data Ready RX FIFO interrupt. Asserted when new data arrives RX FIFO Write 1 to clear bit.
5	0	TX_DS	Data Sent TX FIFO interrupt. Asserted when packet transmitted on TX. Write 1 to clear bit.
4	0	SYNC_DS	RX sync detector interrupt, Write 1 to clear bit. If SYNC_DS is asserted it must be cleared to enable further communication.
3	0	TIMER_INT_STATUS	Timer interrupt status
			1 Timer interrupt is assert

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			0	Timer interrupt is not assert
2	0	RX_TIMEOUT_INT	RX timeout status	
			1	RX timeout interrupt is assert
			0	RX timeout interrupt is not assert
1	0	EVENT_DONE	Event done status	
			1	Event is done
			0	Event is not done
0	0	TX_FULL	TX FIFO full flag	
			0	Available locations in TX FIFO
			1	TX FIFO full

STATE (RW) Address: 08h

The register can NOT be read or written at Standby/PowerDown mode. The value will be lost and can NOT be restored after user wakes up OM6221 to Active mode.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved				CAL_ST_CS			
0				0			
RW				R			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		STATE_CS					
0		0					
RW		R					

Description of Word

Bit	Value	Symbol	Description
15:12	0	Reserved	
11:8	4'b0	Cal_st_cs	Describe the state of calibration state machine
7:6	0	Reserved	Only 0 allowed
			0 Keep the current value
			1 Reset to default values
5:0	6'b0	State_cs	Describe the state of main state machine

CHAN (RW) Address: 09h

The register can NOT be read or written at Standby/PowerDown mode. The value will be lost and can NOT be restored after user wakes up OM6221 to Active mode.

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
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Chan_mn	Reserved	CHAN_FRAC_REG					
0	0	0					
RW	RW	RW					
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
CHAN_FRAC_REG							
0							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CHAN_FRAC_REG							CHAN_INT_REG
0							0
RW							RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHAN_INT_REG							
0							
RW							

Description of Word

Bit	Value	Symbol	Description
31	1'b0	Chan_mn	Channel int and frac part select
			0 Come from the calculation from rf_ch
			1 Come from register
30	2'b0	Reserved	Only 0 allowed
			0 Keep the current value
			1 Reset to default values
29:9	0	CHAN_FRAC_REG	PLL frequency fragment pat
8:0	0	CHAN_INT_REG	PLL frequency integer pat

FDEV (RW) Address: 0ch

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							
FDEV							
0							
0x20							
R							
RW							

Description of Word

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Bit	Value	Symbol	Description
7	0	Reserved	
6:0	7'h20	FDEV	The max offset of the frequency

DAC_RANGE (RW) Address: 0dh

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Bw_dac	DAC_RANGE_REG					
0	0	0					
R	RW	RW					

Description of Word

Bit	Value	Symbol	Description
7	0	Reserved	
6	0	Bw_dac	Control DAC buffer bandwidth
5:0	6'b0	DAC_RANGE_REG	DAC calibration Range control

CTUNING (RW) Address: 0fh

The register can NOT be read or written at Standby/PowerDown mode. The value will be lost and can NOT be restored after user wakes up OM6221 to Active mode.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved			CTUNING_REG_RX				
0			0				
R			RW				
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			CTUNING_REG_TX				
0			0				
R			RW				

Description of Word

Bit	Value	Symbol	Description
15:13	0	Reserved	Only 0 allowed
			0 Keep the current value
			1 Reset to default values

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12:8	6'b0	CTUNING_RE G_RX	AFC coarse tuning register control	
7:5	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
4:0	6'b0	CTUNING_RE G_TX	AFC coarse tuning register control	

FTUNING (RW) Address: 10h

The register can NOT be read or written at Standby/PowerDown mode. The value will be lost and can NOT be restored after user wakes up OM6221 to Active mode.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved					FTUNING_REG_RX		
0					0		
R					RW		
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					FTUNING_REG_TX		
0					0		
R					RW		

Description of Word

Bit	Value	Symbol	Description	
15:11	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
10:8	3'b0	FTUNING_RE G_RX	AFC fine tuning register control	
7:3	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
2:0	3'b0	FTUNING_RE G_TX	AFC fine tuning register control	

RX_CTRL (RW) Address: 11h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
sbe_max_th				xcorr_th[6:2]			

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0	0	1	1	0	1	0	0
RW	RW	RW	RW	RW	RW	RW	RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
xcorr_th[1:0]		en_dc_removal	en_sbe	Rx_tm_mode	Agc_fsync_lock	h_idx	
0	0	1	1	0	0	1	0
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
15:13	3'b001	sbe_max_th	Sync address error tolerance
12:6	7'h50	xcorr_th	Sync threshold
5	1	en_dc_removal	Dc remove enable
4	1	en_sbe	Sbe enable
3	0	Rx_tm_mode	1: rx timeout is count by 32us one bit 0: rx timeout is count by 1us one bit
2	0	Agc_fsync_lock	0: RF_GAIN will not be locked after sync 1: RF_GAIN will be locked after sync
1:0	2'b10	h_idx	modulation index: when 1: 0.32, when 2: 0.50;

FAGC_CTRL_1 (RW) Address: 13h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Reserved			pkdet_vrefc			pkdet_vref2c	
0			3'h2			1	
RW			RW			RW	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reserved	agc_dpd_lo_thr[10:4]						
0	7'h5						
RW	RW						
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
agc_dpd_lo_thr[3:0]				Reserved			Reserved
4'ha				0			0
RW				RW			RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Vco_amp_ctr		Reserved			

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0	10	4'h0
RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
31:29	0	Reserved	
28:26	3'b010	pkdet_vrefc	Pkdetvrefc value
25:24	2'b01	pkdet_vref2c	Pkdet vref2c value
23	0	Reserved	
22:12	11'h05a	agc_dpd_lo_thr	Filter gain low threshold, default 90
11:9	0	Reserved	
8	0	Reserved	
7:6	0	Reserved	
5:4	10	Vco_amp_ctr	VCO amplitude control
3:0	4'h0	Reserved	

W_PLL_LCK_2 (RW) Address: 14h

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W_tx_pll_lck2							
8'h32							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W_rx_pll_lck2							
8'h28							
RW							

Description of Word

Bit	Value	Symbol	Description
15:8	8'h32	W_tx_pll_lck2	W_tx_pll_lck2 can tune TX setup time when bp_calib=1
7:0	8'h28	W_rx_pll_lck2	W_rx_pll_lck2 can tune RX setup time when bp_calib=1

DOC_DACI (RW) Address: 1ah

The register can NOT be read or written at Standby/PowerDown mode. The value will be lost and can NOT be restored after user wakes up OM6221 to Active mode.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-------	-------	-------	-------	-------	-------	-------	-------

OM6221 BLE Register Map v0.7

Reserved	doc_daci
0	0
RW	RW

Description of Word

Bit	Value	Symbol	Description
7	0	Reserved	Only 0 allowed
			0 Keep the current value
			1 Reset to default values
6:0	0	doc_daci	Doc calibrationdaci value

DOC_DACQ (RW) Address: 1bh

The register can NOT be read or written at Standby/PowerDown mode. The value will be lost and can NOT be restored after user wakes up OM6221 to Active mode.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	doc_dacq						
0	0						
RW	RW						

Description of Word

Bit	Value	Symbol	Description
7	0	Reserved	Only 0 allowed
			0 Keep the current value
			1 Reset to default values
6:0	0	doc_dacq	Doc calibration dacq value

AGC_CTRL (RW) Address: 1ch

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
test_pat_en	adp_samp_mode			agc_samp_mode		agc_dpd_mode	agc_dpd_thr_db[5]
0	0	0	0	1	0	0	1
RW	RW	RW	RW	RW	RW	RW	RW
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
agc_dpd_thr_db[4:0]				agc_dpd_thr[10:8]			
1	0	1	1	0	0	1	0

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RW	RW	RW	RW	RW	RW	RW	RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
agc_dpd_thr[7:0]							
1	1	0	0	1	1	1	1
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
23	0	test_pat_en	Test pattern enable
22:20	0	adp_samp_mode	Number of clock cycles delay between every two apd detection: When 0, 0 cycles When 1, 2 cycles When 2, 4 cycles When 3, 8 cycles When 4, 16 cycles When 5, 32 cycles
19:18	2	agc_samp_mode	The number of shift registers which are required for Dpdcaculation. When 0, 2 registers When 1, 4 registers When 2, 8 registers When 3, 16 registers
17	0	agc_dpd_mode	'0': mean of sample amplitudes, '1': max of sample amplitudes;
16:11	6'h36	agc_dpd_thr_db	dB value of agc_dpd_thr minus 3 dB, default 54
10:0	11'h2cf	agc_dpd_thr	Filter gain high threshold, default 719

AGC_GAIN (RW) Address: 1dh

The register can NOT be read or written at Standby/PowerDown mode, the value can be restored after user wakes up OM6221 to Active mode.

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
agc_gain_mn	apd_clr_cnt_th					apd_det_cnt_th[4:3]	
0	0	0	1	1	1	0	0
RW	RW	RW	RW	RW	RW	RW	RW
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
apd_det_cnt_th[2:0]			dpd_clr_cnt_th[5:1]				
1	1	1	0	1	0	1	1
RW	RW	RW	RW	RW	RW	RW	RW
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
dpd_clr_cnt_th [0]	reserved		Agc_apd_state_reg[1:0]		Agc_dpd_state_reg[2:0]		

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1	0	0	0	0	0	0	1
RW	RW	RW	RW	RW	RW	RW	RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Agc_dpd_state_reg[10:3]							
0	0	0	0	0	0	0	1
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
31	0	agc_gain_mn	Agc output gain is get from software or hardware calculation
			1 From software
			0 From hardware
30:26	5'h7	apd_clr_cnt_th [4:0]	Analog Gsw+Gsetl time interval
25:21	5'h7	apd_det_cnt_th [4:0]	Apd detection time interval
20:15	6'h17	dpd_clr_cnt_th [5:0]	DigitalGsw+Gsetl time interval, and add Dpd detection time interval
14:13	2'b00	reserved	
12:11	0	Agc_apd_state_r eg	When agc_gain_mn is 1, the value read from this register is the Lna gain given by the software. When agc_gain_mn is 0, the value read from this register is the Lna gain calculated from the hardware module
10:0	3'b101	Agc_dpd_state_ reg	When agc_gain_mn is 1, the value read from this register is the filter gain given by the software. When agc_gain_mn is 0, the value read from this register is the filter gain calculated from the hardware module

RF_IVGEN (RW) Address: 1eh

Bit23	Bit 22	Bit 21	Bit 20	Bit19	Bit 18	Bit 17	Bit16
Calib_rx_reg	Tx_0_1_rvs	Pd_lna_reg	Pd_lna_mn	Pd_pa_reg	Pd_pa_mn	Tia_lobias	
1	0	0	0	0	0	0	1
RW	RW	RW	RW	RW	RW	RW	RW
Bit 15	Bit 14	Bit13	Bit12	Bit 11	Bit 10	Bit 9	Bit 8
Pd_adc_ldo_re g	Pd_adc_ldo_m n	Pd_mix_reg	Pd_mix_mn	Bm_filter[1:0]		Bm_lna	
0	0	0	0	10		10	
RW	RW	RW	RW	RW		RW	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pa_voltage	Pd_xtal_reg	Pd_xtal_mn	Xtal_cc				
0	0	0	0	1	1	1	1

OM6221 BLE Register Map v0.7

RW	RW	RW	RW	RW	RW	RW	RW
----	----	----	----	----	----	----	----

Description of Word

Bit	Value	Symbol	Description
23	1	Calib_rx_reg	Manual calibration TX/RX select
			1 Manual calibration for RX
			0 Manual calibration for TX
22	0	Tx_0_1_rvs	TX 0/1 reverse
			1 Reverse the 0/1 when transmit
			0 Not reverse
21	0	Pd_lna_reg	Pd_lna manual value
20	0	Pd_lna_mn	Pd_lna manual select
			1 from register
			0 From FSM
19	0	Pd_pa_reg	Pd_pa manual value
18	0	Pd_pa_mn	Pd_pa manual select
			1 from register
			0 From FSM
17:16	1	Tia_lobias	Output to analogue
15	0	Pd_adc_ldo_reg	Pd_adc_ldo manual value
14	0	Pd_adc_ldo_mn	Pd_adc_ldo manual select
			1 from register
			0 From FSM
13	0	Pd_mix_reg	Pd_mix manual value
12	0	Pd_mix_mn	Pd_mix manual select
			1 from register
			0 From FSM
11:10	2'b10	Bm_filter	Filter bias current control
9:8	2'b10	Bm_lna	Output to analogue
7	0	Pa_voltage	Pa voltage output to analogue
6	0	Pd_xtal_reg	Pd_xtal manual value
5	0	Pd_xtal_mn	Pd_xtal manual select
4:0	5'b01111	Xtal_cc	Output to analogue

TEST_PKDET (RW) Address: 1fh

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
test_en	Reserved			Reserved		pll_icp_sel	
0	0			0	1	0	1

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RW	RW			RW	RW	RW	RW
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
test_mode			test_point_sel1			test_point_sel0	
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
xtal_resc		bm_xtal	Reserved	pll_vdiv2_sel		Reserved	Reserved
0	0	1	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description
23	0	test_en	Test mode enable
22:20	0	reserved	
19:18	2'b01	Reserved	
17:16	2'b01	pll_icp_sel	Charge pump current control
15:14	3'b000	test_mode	Test mode select
12:10	3'b000	test_point_sel1	Test point select
9:8	2'b00	test_point_sel0	Test point select
7:6	2'b00	xtal_resc	Resistor value control of xtal bias
5	1	bm_xtal	Xtal bias current control
4	0	Reserved	
3:2	2'b00	pll_vdiv2_sel	Div2 dc bias control
1	0	Reserved	
0	0	Reserved	